3-11-81
ML- 3

Mod#	ECO#	Date Issued	CHANGE	REASON
1	359	7-30-80	Addition of 33pf cap across (parallel to) R19. (Component Side)	When a 16KTP has as Q1 a CDC 2N3646 and is operating warm to hot, the combined delays of the 'LS' parts and the CDC 2N3646 are such that the PRDY line is not pulled low in time for a Z80 WAIT state to occur. The result is that the HOST write is not done (nothing is written to the 16KTP).
2	400	9-2-80	Change IC3 from 74LS04 to 74S04. Change IC57 from 74LS86 to 74S86. Change IC74 from 74LS08 to 74S08. Change IC75 from 74LS125 to 74125.	To speed up $\overline{MEMDISABLE}$ circuitry to be compatible with the 64KZ Rev.J card.
3	661	3-11-81	Change IC8 from a 74125 to a 74LS125. Change R1 from 180Ω to 390Ω. Add a 390Ω resistor between IC59-1 & IC59-14 (+5V).	Assorted fan-out problems.

3-3-80

Mod#	ECO#	Date Issued	CHANGE	REASON
1	252	5-14-80	Various modifications; see the ECO, p.2, for details.	Corrections to Rev. E board.
2	288 428	6-12-80 9-24-80	On solder side: 1. Jump IC74-3 → IC3-5. Jump IC3-6 → IC75-2. 2. Jump IC74-1 → IC59-4. Jump IC74-2 → IC58-10. 3. Cut trace IC40-5 → IC75-2 (on solder side, under C14). See the ECO's for diagram & schematic.	Required to allow $\overline{MEMDSBL}$ to go active in time to disable Host memory access.
3	359	7-30-80	Addition of 33pf cap across (parallel to) R19. (Component Side)	When a 16KTP has as Q1 a CDC 2N3646 and is operating warm to hot, the combined delays of the 'LS' parts and the CDC 2N3646 are such that the PRDY line is not pulled low in time for a Z80 WAIT state to occur. The result is that the HOST write is not done (nothing is written to the 16KTP).
4	400	9-2-80	Change IC3 from 74LS04 to 74S04. Change IC57 from 74LS86 to 74S86. Change IC74 from 74LS08 to 74S08. Change IC75 from 74LS125 to 74125.	To speed up $\overline{MEMDISABLE}$ circuitry to be compatible with the 64KZ Rev. J card.
5	661	3-11-81	Change IC8 from a 74125 to a 74LS125. Change R1 from 180Ω to 390Ω. Add a 390Ω resistor between IC59-1 & IC59-14 (+5V).	Assorted fan-out problems.

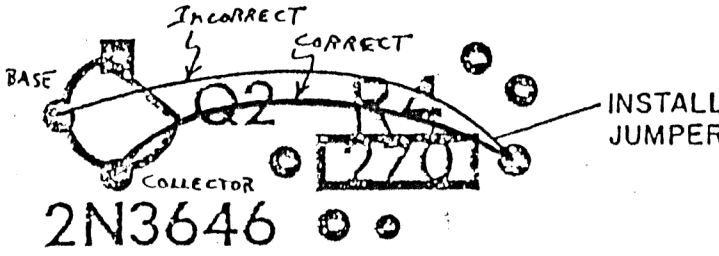| Mod#	ECO#	Date Issued	CHANGE	REASON
1	359	7-30-80	Addition of 33pf cap across (parallel to) R19. (Component Side)	When a 16KTP has as Q1 a CDC 2N3646 and is operating warm to hot, the combined delays of the 'LS' parts and the CDC 2N3646 are such that the PRDY line is not pulled low in time for a Z80 WAIT state to occur. The result is that the HOST write is not done (nothing is written to the 16KTP).
2	400	9-2-80	Change IC3 from 74LS04 to 74S04. Change IC57 from 74LS86 to 74S86. Change IC74 from 74LS08 to 74S08. Change IC75 from 74LS125 to 74125.	To speed up $\overline{MEMDISABLE}$ circuitry to be compatible with the 64KZ Rev.J card.
3	433	2-10-81	Cut the trace leading from IC42-8, component side. Jump IC43-15 → IC26-8, solder side.	Artwork correction. Necessary for proper operation if PROM is used.
4	661	3-11-81	Change IC8 from a 74125 to a 74LS125. Change R1 from 180Ω to 390Ω. Add a 390Ω resistor between IC59-1 & IC59-14 (+5V).	Assorted fan-out problems.

8-28-80)
ML- 2

Mod#	ECO#	Date Issued	CHANGE	REASON
1	235	5-7-80	Rewire 2 sections of IC15 (74LS175) per marked print. (see Eco, p.2) Change IC44 from an S374 to LS374. Change IC15 from 74LS175 to 74175.	Reduces clock rate on state logic to improve high temp operation and allow for propogation delays.
2	392	8-28-80	Change R2 from 560Ω to 220Ω and R5 from 560Ω to 220Ω. Change C1 from 47pf mono to 100pf mono and C10 from 100pf mono to 220 pf mono. Change IC7 from 74LS00 to 74S00 and IC65 from 74LS11 to 74S11.	Interaction with 64KZ Rev.J caused INVALID JUMP'S to occur, because MEMDISABLE was being released too late. This change speeds up the MEMDISABLE circuit on the 48KTP by 22 nsec.

Mod#	ECO#	Date Issued	CHANGE	REASON
1	392	8-28-80	Change R2 from 560Ω to 220Ω and R5 from 560Ω to 220Ω. Change C1 from 47pf mono to 100pf mono and C10 from 100pf mono to 220pf mono. Change IC7 from 74LS00 to 74S00 and IC65 from 74LS11 to 74S11.	Interaction with 64KZ Rev.J caused INVALID JUMP'S to occur, because MEMDISABLE was being released too late. This change speeds up the MEMDISABLE circuit on the 48KTP by 22 nsec.
2	545	1-16-81	1. Remove C24 (22pf mono capacitor). 2. Replace R6 (270) with a wire.	To provide compatibility with PAL version of the SDI board set.

Mod#	ECO#	Date Issued	CHANGE	REASON
1	228	5-2-80	1. Change IC3 from 74LS74 to 7474. 2. a. Change R6 from 1K resistor to 2.2K 1/4 watt 5% resistor. b. Change IC34 from 7474 to 74LS74.	1. To provide sufficient drive current to the ϕ clock on Z80. 2. To decrease load on priority chain.
2	275	6-3-80	Change R1 from 4.7K to 1K.	Stiffer pull-up improves waveform at processor/WAIT input.
3	377	8-20-80	Cut trace connecting IC1-2 to IC1-3. Cut trace connecting IC1-3 to R14. Cut trace connecting R14 to R15. Jumper the now unconnected end of R15 to IC1-3. Jumper the unconnected end of R14 to IC1-2. Solder a .001μf (004-0043) from the jumper end of R14 to the jumper end of R15.	By AC coupling between inverters, inverter 2 will self bias its input to the threshold value. This causes better oscillator start up and stability with worst case LS04's.
4	383	8-21-80	Cut the solder side trace connecting IC2-2 to the adjacent plate-through-hole. Jumper IC2-2 to IC32-8, majority of jumper on component side.	The flip-flop controlling the $\overline{INT}$ line of IOP Z-80 will not relinquish the $\overline{INT}$ on an interrupt acknowledge cycle without this change.
5	389	8-26-80	Solder a 1K pullup between IC39-15 and IC39-20, a 74LS244.	Documentation states that D5 of the IOP flag port will always be a "1". At present, the input to that buffer is floating.
6	425	9-17-80	Cut traces coming from pins 9 and 13 of IC36. Jump IC36-9 → IC42-16, & IC36-13 → IC42-11.	50ns low pulses occur on $\overline{CBUSCLR}$ and $\overline{CLRBUSY}$ when they should remain high, (when writing with D5=0 to the control port and writing with D1=0 to the status port, respectively).

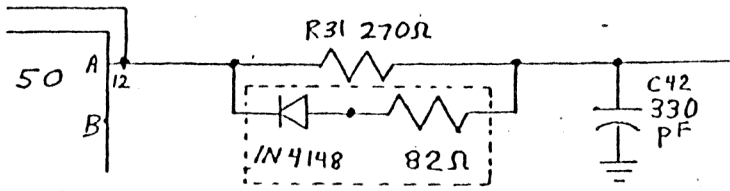| Mod#	ECO#	Date Issued	CHANGE	REASON

7	513	12-10-80	PCB Assy: Delete-
			
			  Q5 2N3646 transistor 009-0000
			  R16 1 KOHM resistor 001-0018
				These components are part of the pRDY circuit which has been eliminated.

8	514	12-10-80	On solder side:
			
			  Jump IC41-10 → IC56-2,
			  Cut trace between IC56-2 & IC37-8,
			    next to IC56-2.
				This changes the "STAT FULL" bit from hardware to software control.

Mod#	ECO#	Date Issued	CHANGE	REASON
1	30	7/16/79	Remove transistor Q2, Remove resistor R4 (optional), Install jumper between IC25-3 side of R4 → collector side of Q2. *Note that diagram in manual (Jul. '79) is incorrect:	
3	632 Prod. only	2-25-81	RN1, RN5, RN8, RN11, RN14: Change from 10K 9 res 10 pin SIP to 5.6K SIP R-Net.	The MTC-66 opto-isolator has a minimum 6% current transfer ratio but has no upper limit. This no upper limit CTR causes a very slow turn off of the high CTR opto-isolator, that in turn causes some devices (about 10%) to fail the timing specifications for turn off -i.e. rise-time of the signal at the collector of the device. This value will decrease the turn off time, providing a value closest to the minimum practical. The net result should be fewer devices failing because of high CTR.
2	57	9/16/79	Cut pin 26 of 26-pin CA connectors.	Polarizing key added to all cables attached to these connectors, to guarantee correct mating of cable to connector.

Mod#	ECO#	Date Issued	CHANGE	REASON
1	10	4-9-79	1) Cut trace to IC37-4 and jump from this pin to Ground. 2) Cut trace to IC37-6 and jump from this pin to IC40-5.	These changes make the output strobe timing agree with that shown in the manual.
2	11	4-10-79	IC11 should be a 74LS244.	Legend mask in error.
3	35	7-27-79	Changes to schematic. (See ECO)	Errors.
4	57	11-16-79	Cut pin 26 of 26 Pin CA connector.	Polarizing key will be added to the cables attached to this.
5	706	3-31-81	IC31 should not be a TI 74LS04. Other vendors (National, etc.) will suffice. P/N 010-0066.	TI 74LS04 is too sensitive to ground spikes, which can cause false latching of the input latched status flip-flops.

Mod#	ECO#	Date Issued	CHANGE	REASON
1	706	3-31-81	IC31 should not be a TI 74LS04. Other vendors (National, etc.) will suffice. P/N 010-0066.	TI 74LS04 is too sensitive to ground spikes, which can cause false latching of the input latched status flip-flops.

3-3-80

Mod#	ECO#	Date Issued	CHANGE	REASON
1	357	8-7-80	Replace metal screw & washer with nylon screw & washer at the heatsink of IC28, a 7905C.	The heatsink of this regulator is electrically hot. The nylon hardware will alert users to this fact.

2-3-80

Mod#	ECO#	Date Issued	CHANGE	REASON
1	432	9-29-80	Across R31, add an 82Ω resistor in series with a 1N4148 diode, with N side of diode facing IC50. schematic:	Needed for compatibility with 64KZ Rev.J. Enables high-to-low propogation delay from IC50-12 to IC67-7 to equal the corresponding low-to-high propogation delay. Previously, AØ was too slow in going from a high-to-low transition.

3-3-80

Mod#	ECO#	Date Issued	CHANGE	REASON
1	000	8-10-78	Cut trace to IC9-5 (+5V tie). Jump IC9-5 → IC9-7. (Socket must be removed to effect this change.)	IC9-5 should be tied to Ground, not to +5V.
2	357	8-7-80	Add longer nylon screw (1/2") and nylon washer to heatsink of IC2 (a 7905).	The heatsink of this regulator is electrically hot. Addition of the nylon hardware will alert users to this fact.
3 In Effect 5-6-81	211	4-21-80	1) Cut trace connecting cathode of D1 to IC26-5. ANODE D1 CATHODE CUT HERE Jump IC1-3 → D1 cathode. (PC Assy: jumper should be via component side)	When the bank enable switch is off, LED D1 is off, indicating that the board is disabled, when in reality it is enabled. This fix corrects this: LED should be on when board is enabled.
	246	5-13-80	2) Change IC1 from 74LS00 to 7400, change IC26 from 7474 to 74LS74.	The output of IC1-3 (an LS part) is not capable of driving the LED D1, as per ECO 211. Changing IC1 to a TTL part will increase the drive current. IC26 may be changed to an LS part because the LED is now being driven by IC1.

Mod#	ECO#	Date Issued	CHANGE	REASON
1	50	10-30-79	Insert a 22Ω resistor between D6 and T1-5 of the 26V DC to DC program power supply. The connecting trace between these two terminals must be cut also.	The 22Ω resistor limits the surge current from transistor, Q1, into filter cap, C3, when the board is powered up with the PROGRAM POWER switch in the ON position. The reduced load on Q1 improves the power supply reliability.
2	144	3-7-80	Change D5 to D4 on legend and schematic. Change D6 to D5 on legend & schematic. Reverse DMA IN/OUT and DMA ENABLE labeling on address/control switch on the legend.	To correct reference #/labeling errors.

Mod#	ECO#	Date Issued	CHANGE	REASON
1	144	3-7-80	The legend indicates two R18 resistors. Change the one next to C5 to R19 on legend and schematic.

Change D5 to D4 on legend & schematic.

Change D6 to D5 on legend & schematic.

Reverse DMA IN/OUT and DMA ENABLE labeling on address/control switch on the legend. | To correct reference #/labeling errors. |
| 2 | 145 | 3-7-80 | Cut trace leading from resistor network RN5, pin 5, on component side. | RN5-5 (1K) was supposed to be a pull-up for IC19-4 (74LS05). However, this output is pulled up by RN1-10 (4.7K). Disconnecting RN5 reduces the load on the 74LS05. |

3-3-80

Mod #	ECO #	Date Issued	CHANGE	REASON
1	24	7-2-79	Insert deglitching RC filter on PHLDA R= 220 Ω C= 150 pf.	Filter prevents noise on pHLDA from causing unwanted DMA cycles.
2	357	8-7-80	Longer nylon screw (1/2') and nylon washer added to each heatsink of IC11 (7905C) and IC12 (7905C).	These heatsinks are electrically hot. Use of the nylon hardware will alert users to this fact.

3-3-80

Mod#	ECO#	Date Issued	CHANGE	REASON
1	357	8-7-80	Longer nylon screws (1/2") and nylon washers added to heatsinks of IC11 (7905C) IC12 (7905C).	These heatsinks are electrically hot. Use of the nylon hardware will alert users to this fact.

3-3-80