BOARD MODIFICATIONS for 4FDC REV C

ML-7
7-28-80

Mod#	ECO#	Date Issued	CHANGE	REASON
1	1	1-5-79	IC6 is changed from a 74368 to a 8T98N.	
2	3	2-8-79	IC17 changed from 74LS02 to 7402.	Schottky part would not drive all loads connected to it.
3	31	7-16-79	Jumper J2-2→IC14-7 (via J3-32), for maxi. Jumper J3-32→IC14-7 (via J4-21), for the mini.	To use the 4FDC with a double-sided disk drive, the side select input to the drive must be accessed through Port 4 (the auxilliary disk command).
4	44 47	9-12-79	Cut trace from J3-14→J2-4 (DS3). Jump IC10-9→J2-18 (DS4), (via J3-14). Cut trace IC10-3/J3-6→J2-18 (DS4). Jump IC10-3→J2-4 (DS3), (via J3-6).	The model 299B drive select pins DS3 & DS4 are reversed from those on the model 277. Therefore, when used with a 4FDC, drives 'C'& 'D' will be reversed from their customary positions in a CS-3. To correct this the drive select pins DS3 & DS4 must be interchanged on the 4FDC.
5	56 57	9 -16-79	Cut pin 17 of 34-pin CA connector, J3, (# 017-0013). Cut pin 13 of 50-pin CA connector, J2, (# 017-0014). Cut pin 26 of 26-pin CA connector, J4, (# 017-0012).	A polarizing key will be added to cables attached to these connectors to guarantee correct mating.
6	140 superseded ECO(169)	3-3-80	IC's 42, 45, 46: Change from 74367 to National 80L97. This change eliminates the need for the four 0.001μf caps on the outputs of IC46 (Address buffer). Also remove the two 47pf caps on IC43.	80L97 is slower than 74367 and therefore eliminates noise on the address and control lines on the 4FDC. Noise on the address lines causes IC23 (ROM) to glitch on pins 2,3,4,5 and 7 (especially at 2 MHz). These glitches are transmitted to the address and SYNC pins of the TMS5501 causing it to malfunction.

Mod#	ECO#	Date Issued	CHANGE	REASON
7	169	3-31-80	The changes here supercede ECO #140, except that the two caps on IC43 remain off. Either use 80L97 for IC45 and IC46, OR attach .001 µf caps from pins 8 (GND) to IC45 pins 3,5,7,11, and IC46 pins 3,5,7,9,13. Cut IC42 pins 6&7 directly on the plastic dip package. Use a 74367 for IC42. Jump IC42-6 → IC46-14. Jump IC42-7 → IC46-13. Add .001 µf from IC46-13 → IC46-8. If IC46 is not 80L97. Jump IC46-1 → IC46-15.	Noise must be filtered from S-100 bus inputs A7, A6, A5, A4, A3, A2, A1, A0, and PDBIN. This is done by using either a slower IC (the 80L97) or by attaching .001 µf capacitors between GND and the outputs of the buffers for these bus inputs. Since changing IC42 to an 80L97 can create problems on the PRDY line in multi-user systems, we disconnect the PDBIN line from the IC42 buffer and tie it in to a free buffer on IC46 (which must also be grounded through pin 15).
8	203	4-18-80	Install a 1K resistor between IC49-1 & IC49-16, on the component side.	This is a pull-up resistor which acts to ensure a fast transition from low to high on the output of IC23-7 when the chip is deselected.
9	334	7-15-80	Metal screw in REG. 7905/320T-5 to be changed to nylon screw.	Customers have often damaged their equipment by using the metal screw as a grounding point.

BOARD MODIFICATIONS for 4FDC REV E

10-17-80

ML-2

Mod#	ECO#	Date Issued	CHANGE	REASON
1	452	10-10-80	Jump IC53-13 → +5V.	Artwork change; IC53 pin 13 is floating.
2	448	10-9-80	R17 should be 5.6K resistor, not 100Ω	Legend in error.

BOARD MODIFICATIONS for 16FDC REV E

12-11-80

ML- 7

Mod#	ECO#	Date Issued	CHANGE	REASON
1	315	7-7-80	1. Change IC14 from a 74LS04 to a 7404. 2. Change C20 from 30pf to .005μf.	1. The 74LS04 is more susceptible to overtone frequencies due to its speed characteristics. 2. C20 should be changed to match the oscillator circuit on the ZPU.
2	302	6-23-80	IC4-4 must be tied to +5V.	IC4-4 is floating.
3	334 387	7-15-80 8-25-80	Metal screw in Reg. 7905/320T-5 to be changed to nylon screw. Lockwasher (metal) to be used.	Customers have often damaged their equipment by using the metal screw as a grounding point.
4	335 387 424	7-15-80 8-25-80 9-19-80	On the 7805C Regulator, use a 6-32 X 5/8 metal screw in combination with a nylon shoulder washer on the solder side.	To prevent shorting with adjacent trace on solder side.
5	345	7-29-80	Replace the 300pf capacitor at C21 with a 75pf capacitor. (See ECO for schematic)	The larger value capacitor will sometimes cause so much delay that the clocks into the 5501 lose their timing relationship. This causes the 5501 to ignore serial receive data and not start RDOS.
6	384	8-22-80	Change R1 from 5.62K to 5.49K.	To improve the free running frequency of the data separator for small double density drives.
7	520	12-11-80	Replace the 74LS367 at IC13 with a 74367 (standard TTL part).	Bus contention on the 16FDC between IC26 and IC49 at the trailing edge of the $\overline{RE}$ pulse causes glitching at these outputs. The 74367's have higher V_{IL}, and are therefore less susceptible to noise glitches. This problem observed so far in board test and not in the field.

BOARD MODIFICATIONS for 16FDC REV F1 Date 3-24-81

ML 2

Mod#	ECO#	Date Issued	CHANGE	REASON
1	596	2-10-81	On component side, add wire from plate-through hole near J3 pin 50 to top side of R20. (see ECO for diagram)	Missing trace; +12V not connected to IC16, the ϕ_1 & ϕ_2 generation circuit, R5, R6 & R20.
2	695	3-26-81	R7 should be a 10K resistor. Solder mask must be scraped off before soldering.	Solder mask, legend error.

BOARD MODIFICATIONS for 16KZ REV C

Date 2/25/81

ML 3

Mod#	ECO#	Date Issued	CHANGE	REASON
1	-	1979?	Insert three 1.5K resistors as follows: between RN2-8 & IC34-16 (+5V) between IC34-9 & BB side of C45 (+5V) & between IC51-9 & RN14-1 (+5V).	To pull up lines for faster switching.
2	25	7/2/79	Add 1.5K resistor between +12V regulated supply & Ground.	Problem occurs when used with IMI drive. When the RAM array is disabled during DMA, there is not enough current drawn from the +12V regulator to maintain constant output voltage. Consequently, random bits in memory are lost. The 1.5K bleeder resistor loads the regulator so that its voltage remains constant.
3	630	2/25/81	Replace R24, a 2.2K resistor, with a 680Ω resistor, 1/2 Watt.	To provide sufficient bias current for the 1N5231 Zener diode on the -18V line.

BOARD MODIFICATIONS for 16KZ REV D Date 2-25-81

ML 2

Mod#	ECO#	Date Issued	CHANGE	REASON
1	25	7/2/79	Add 1.5K resistor between +12V regulated & Ground.	Problem occurs when used with IMI drive When the RAM array is disabled during DMA, there is not enough current drawn from the +12V regulator to maintain constant output voltage. Consequently, random bits in memory are lost. The 1.5K bleeder resistor loads the regulator so that its voltage remains constant.
2	630	2/25/81	Replace R24, a 2.2K resistor, with a 680Ω resistor, 1/2 Watt.	To provide sufficient bias current for the 1N5231 Zener diode on the -18V line.

Mod#	ECO#	Date Issued	CHANGE	REASON
8	142	3-3-80	1. Cut trace between IC57-5 & IC21-4/IC21-12 on component side. 2. Cut trace between IC57-5 & IC54-12, solder side. 3. Add 180Ω resistor between IC57-5 & IC54-12 on the component side. 4. Install 220pf cap between IC54-12 & end of IC72 (regulator, middle pin), component side. 5. Jump IC54-12 → IC21-4, solder side.	This eliminates the chance of glitch on IC57-5 (Q output) feedback to the J input of IC57 through IC's 54, 5, and 36. The glitch is caused by occurance of a clock to IC57 during data set-up time. In effect, it causes the memory to miss a write cycle.
9	471	10-27-80	1. Change R21 from 330Ω resistor to 1K resistor. 2. Change R7 & R8 from 2.2K resistors to 680Ω resistors.	1. IC25 (an LS25 part) fanout exceeded. The IC tries to sink 17mA w/c. 2. Stiffer pullups (faster risetimes on bank select circuit).

BOARD MODIFICATIONS for 64KZ REV G1, G2 ML- 5
Date 11-14-80 * ECO 380 ADDED

1	43	9-6-79	IC37 changed from 74LS74 to 7474.	Load on pin 9 is handled better.

Mod#	ECO#	Date Issued	CHANGE	REASON
2	141	3-3-80	1. Cut trace between Z55-2 and Z3-3 on the component side. 2. Install a 220Ω resistor between Z55-? and Z3-3 on the component side. 3. Install a 150 pf capacitor between Z3-3 and Z3-7 on the component side. ****This supercedes ECO 93. Either the trace between Z36-8 and Z58-9 on the pin side should be un-cut, or there should be a continuous jumper between Z36-8 and Z58-9. No jumpers to IC 56, (FF).	This eliminates the glitch on the output of Z55-2 due to occurance of a clock to Z55 during data set-up time. It also suppresses glitches transmitted from Z57-15 during SMEMR cycle.
3	142	3-3-80	1. Cut trace between Z57-5 and Z21-4/ Z21-12 on the component side. 2. Cut trace between Z57-5 and Z54-12 on the pin side. 3. Install a 180Ω resistor between Z57-5 and Z54-12 on the component side. 4. Install a 220 pf capacitor between Z54-12 and end of Z72 (regulator, middle pin) on the component side. 5. Install jumper between Z54-12 and Z21-4 on pin side.	This eliminates the chance of glitch on Z57-5 (Q output) feedback to the J input of IC57 through IC's 54, 5, and 36. The glitch is caused by occurance of a clock to IC57 during data set-up time. In effect, it causes the memory to miss a write cycle.
1.5	106	2-6-80	IC's 55,56,76: Replace 74S374 with 54S374.	Higher temp. range, more reliable.
4	471	10-27-80	1. Change R21 from 330Ω resistor to 1K resistor. 2. Change R7 & R8 from 2.2K res to 680Ω resistors.	1. IC25 (a 74LS25 part) fanout exceeded. The IC tries to sink 17mA w/c. 2. Stiffer pullups (faster risetimes on bank select circuit).

2-3-80

Mod#	ECO#	Date Issued	CHANGE	REASON
5	380	8-20-80	Change R12 from 2.7K to 4.7K.	To guarantee, that, on reset, IC23-12 is pulled to a valid low.

J. Miller

BOARD MODIFICATIONS for G4KZ REV J, J1

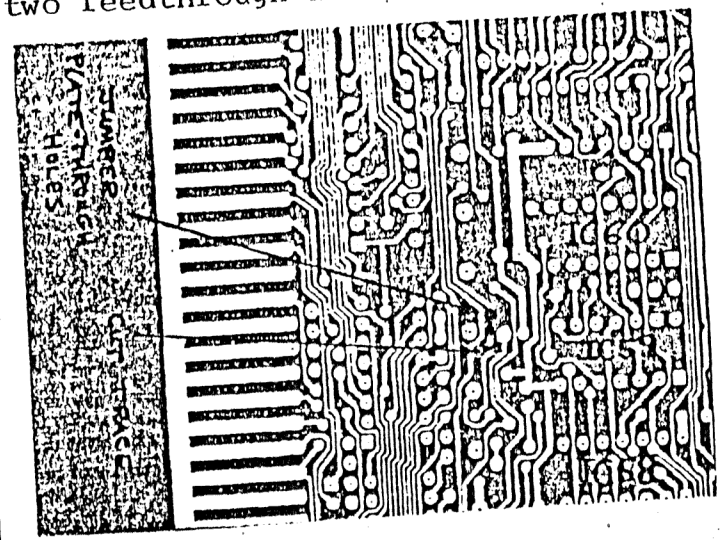
ML- 10
Date 6-1-81

Mod#	ECO#	Date Issued	CHANGE	REASON
1	379	8-20-80	Change IC77 from 74LS374 to 74LS373.	Considering a worst case ZPU-data from the ZPU (in a write cycle) is not stable on the rising edge of the clock to IC77, causing incorrect data to be written to the memory. Using a transparent flip-flop gives more time for this data to stabilize since it is only sampled when $\overline{CAS}$ goes low.
2	380	8-20-80	Change R12 from 2.7K to 4.7K.	To guarantee, that on reset, IC23-12 is pulled to a valid low.
3	381	8-20-80	Change IC56 from 74LS14 to 74S04. Change R36 from 820Ω to 100Ω. Change R37 from 1.8KΩ to 390Ω. Change C82 from 330pf to 1Kpf.	IC56 was used incorrectly in the Johnson counter and had a fanout problem. IC56 was replaced by S04 and corresponding changes in R-C values were made to compensate for this change since two gates of IC56 are also used in the DMA control circuitry.
4	382	8-20-80	Change C13 from 100pf to 220pf and R10 from 240Ω to 100Ω. Change R11 from 270Ω to 150Ω. Change R9 from 470Ω to 220Ω. Change R35 from 270Ω to 220Ω and C81 from 220pf to 330pf.	R-C network changed to conform with the worst case Schottky input characteristics.
5	420	9-9-80 10-2-80 in effect	Change C59 from 220 pf mono cap to 470 pf mono cap.	Compatibility with 48KTP: This RC fix slows down the start of an M-1 cycle by 18ns (21ns → 39ns propogation delay from IC20-5 to IC21-6) so that $\overline{MEMDISABLE}$ will be clocked in when valid at the 74LS175, IC41. Ref. ECO 400.

BOARD MODIFICATIONS for 64KZ REV J,J1

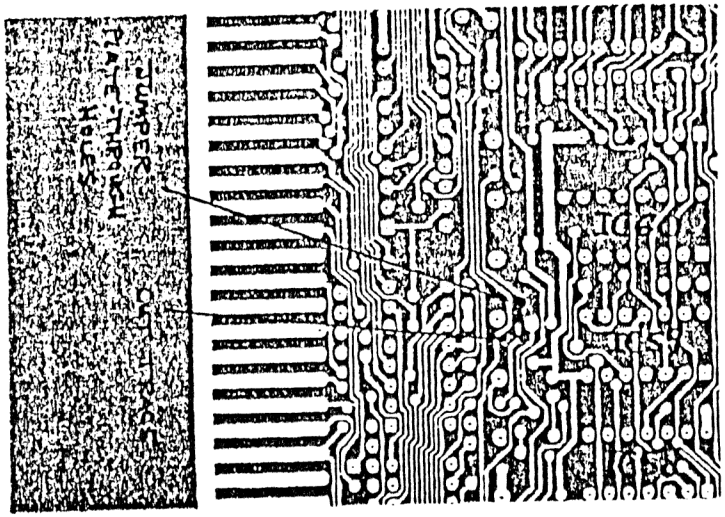
Mod#	ECO#	Date Issued	CHANGE	REASON
6	471	10-27-80	1. Change R21 from 330Ω resistor to 1K resistor. 2. Change R7 & R8 from 2.2K res to 680Ω resistors.	1. IC25 (a 74LS25 part) fanout exceeded The IC tries to sink 17mA w/c. 2. Stiffer pullups (faster risetimes on bank select circuit).
7	378 481	8-20-80 Effective 10-30-80	Remove IC17, R26, R27, L1, and C24. Replace IC55 with the Delay Line package (from Bel Fuse).	All control signals (internal to the 64KZ) are synchronized with the start of any cycle eliminating the 50 nsec jitter generated by the asynchronous on board clock. In the worst case, it makes each cycle faster by 30 nsec.
	615	4-24-81 IN EFFECT	Delete crystal.	Not needed.
	488	11-11-80	Remove IC17 socket, PC assy.	Not needed.
8	505	11-20-80	Change IC76 from a 74S374 to a 54S374.	The failure rate of 74S374's in this application is high as it runs hot. Test jig measurements indicate that the 54S374's will alleviate this component as a source of failure.
9	517	12-12-80	Replace R4 & R5 180Ω resistors with 470Ω resistors.	The LS outputs at IC8 (a 399) could not pull down the diode resistor network in the worst case (which would give erroneous indication of bank activity). The LED's will be dimmer but acceptable.

BOARD MODIFICATIONS for 64KZ REV J, J1

Mod#	ECO#	Date Issued	CHANGE	REASON
10	762	6-1-81	On solder side, cut trace and jump the two feedthrough holes as shown. 	This will route sOUT through the deglitching RC network (RN5 & C69) to IC59-10. Noise on sOUT taken directly off the bus could generate an invalid bank select pulse to IC8-9, causing the system to crash, when writing to memory addresses with lower address of 4ØH (also the bank select port).

* legend J2 Rev.: no "IC17", but "20 MHz" still present.

BOARD MODIFICATIONS for 64KZ REV Solder side: J1
Legend: J2 Date 6-1-81
ML 2

Mod#	ECO#	Date Issued	CHANGE	REASON
1	615	2-18-81 4-24-81 IN EFFECT	Delete 20 MHz Crystal, 026-0002, from board.	Not needed. Delay line is now used.
2	762	6-1-81	On solder side, cut trace and jump the two feedthrough holes as shown. 	This will route sOUT through the de-glitching RC network (RN5 & C69) to IC59-10. Noise on sOUT taken directly off the bus could generate an invalid bank select pulse to IC8-9, causing the system to crash, when writing to memory addresses with lower address of 4ØH (also the bank select port).

BOARD MODIFICATIONS for PRI REV B

3-24-80
ML-4

Mod#	ECO#	Date Issued	CHANGE	REASON
1	6	3-6-79	Insert a 22Ω resistor between IC4-19 and J1-22 (26 pin connector).	Pin 19 of IC4 is the data strobe to the 3703 printer. Without any termination the data strobe has a ringing problem which causes some printers to sporadically print a smudge in column 1. A 22 resistor in series with the strobe output properly terminates the line and eliminates the smudging problem.
2	57	11-16-79	Cut pin 26 of 26 pin CA connectors (#017-0012).	A polarizing key will be added to all cables attached to these connectors.
3	77	12-28-79	IC1, IC2, & IC3 are 74S373, not 74LS373 as indicated on board silk-screen.	The Schottky driver sinks more current than the low power driver which it replaces. The increased current drive is required for 3355A printers.
4	-	3-24-80	In multi-user systems a 4-position addr. DIP switch should be added to the board and the cross-traces cut on the pin side. In a single-user system the switch should not be added and traces should not be cut. (If switch is present, traces must be cut).	When a PRI is present in a multi-user system it must be re-addressed (to FØ) to prevent conflicting addresses with the Tu-Arts in the system.

BOARD MODIFICATIONS for PRI REV E

3-24-80
ML-3

Mod#	ECO#	Date Issued	CHANGE	REASON
1	151	3-18-80	Remove the 7402, IC8, and replace with a 74LS33. Add a 330Ω resistor between IC8-4 and IC8-14 (+5V). Add a 330Ω resistor between IC8-10 and IC8-14 (+5V).	The 74LS33 which replaces the 7402 is an open-collector device that provides more drive to the $\overline{\text{PINT}}$ line.
2	157	3-21-80	RN5 should be 330Ω resistor network. RN6 should be 220Ω resistor network. Also, 3703 & 3779 interrupt address should be 34, and 3355A should be 5C.	Incorrect silkscreen on PCB.
3	159	3-24-80	Cut all (9) cross-traces of the two switch arrays (pin side).	Incorrect artwork.

BOARD MODIFICATIONS for PRI REV D1

3-24-80
ML-2

Mod#	ECO#	Date Issued	CHANGE	REASON
1	151	3-18-80	Remove the 7402, IC8, and replace with a 74LS33. Add a 330Ω resistor between IC8-4 and IC8-14 (+5V). Add a 330Ω resistor between IC8-10 and IC8-14 (+5V).	The 74LS33 which replaces the 7402 is an open-collector device that provides more drive to the $\overline{\text{PINT}}$ line.
2	158	3-24-80	Numerous items; see the ECO itself.	Corrections to schematic and artwork.

3-30-81

M1-8

BOARD MODIFICATIONS for TU-ART REV E

Mod#	ECO#	Date Issued	CHANGE	REASON
1	33 [659] SUPERSEDES	7-19-79	For Tu-Arts used in time-sharing systems: Cut trace IC7-5 → J3-22, and insert a 22Ω resistor between these two terminals.	Pin 7 of IC5 is the data strobe to the 3703 printer. Terminating this output with 22Ω reduces ringing which may cause the printer to print extraneous characters. This change applies only to Tu-Arts which are used to drive 3703 printers.
2	57	11-16-79	Cut pin 26 of 26 pin CA connectors (# 017-0012).	A polarizing key will be added to all cables attached to these connectors to guarantee correct mating of cable to connector.
3	162 [442] Supercedes	3-26-80	D2: Replace 1N914 with a 1N5711, (H.P. #5082-2800). IC34: Replace 74LS00 with a 7400.	To insure a logical 0 level at the circuit node feeding RN1-5, RN1-11, IC34-5, IC10-6, and D2 anode. This provides for proper operation of the priority chain with a greater number of vendors' parts.
4	355	8-6-80	Put 1K resistor between IC24-10 and IC24-14. Put 1K resistor between IC42-1 and IC42-14. Put 1K resistor between IC1-13 and IC1-16.	To pull up outputs of IC28 (74S288) when Tu-Art is not being addressed and the 288 is tri-stated (See ECO 203).
5	357	8-7-80	Replace metal screws & washers with nylon screws & washers, at the locations indicated: IC37-7905/7946	This regulators heatsink is electrically hot. Nylon hardware will alert users to this effect.

Mod#	ECO#	Date Issued	CHANGE	REASON
6	442	10-3-80	(Supercedes ECO 162) Remove D2, pull IC34 pin 5. Jump IC13-12 → IC10-6. Jump IC13-13 → IC13-2. Jump IC13-11 → IC34-5 on the chip. IC34: replace the 7400 with 74LS00.	To improve input thresholds for the worst case in the interrupt priority chain. This change replaces equivalent DTL "AND" function with TTL logic. The 74LS00 is preferable to the 7400.
7	659	3-11-81	R28: Change from 22Ω resistor to 47Ω . To be done on all Tu-Arts.	R28 is added in series to the Data Strobe line (D7) to reduce ringing when a Centronics printer is used (port B). R28 value should be 47Ω, 22Ω is insufficient.
8	681	3-30-81	All 74LS04's should be TI Only. New part no. 010-0066-1.	Chips other than TI fail to oscillate (which oscillation depends on change of gain in linear region).

BOARD MODIFICATIONS for Tu-Art REV H1 Date 3-30-81

ML 2

Mod#	ECO#	Date Issued	CHANGE	REASON
1	659	3-11-81	R28: Change from 22Ω resistor to 47Ω . Should be done on all Tu-Arts.	R28 is added in series to the Data Strobe line (D7) to reduce ringing when a Centronics printer is used (port B). R28 value should be 47Ω , 22Ω is insufficient.
2	681	3-30-81	All 74LS04's should be TI Only. New part no. 010-0066-1.	Chips other than TI fail to oscillate (which oscillation depends on change of gain in linear region).

BOARD MODIFICATIONS for WDI REV D

ML-11
7-25-80

Mod#	ECO#	Date Issued	CHANGE	REASON
1	55	9-6-79	Cut pin 4 of 34 pin connector.	A polarizing key will be added to the WDI cable attached to this connector.
2	76	12-17-79	R17 must be 100Ω, not 680Ω.	680Ω prevents the hard disk from operating with multi-user systems having 5 or more memory cards.
3	81	1-9-80	Jump IC4-6 → IC4-11. Jump IC24-4 → IC24-14. Jump IC18-7 → IC19-7.	Missing artwork.
4	82	1-9-80	Traces to RN6-1 cut on pin side. Jump RN6-1 → IC36-16. Jump RN6-3 → IC37-15. Jump RN6-3 → IC43-15.	Incorrect artwork.
5	83	1-9-80	Pin 11 of IC47 removed from socket. 560Ω between pin 18 of IC45 and pin 11 of IC47 (on component side). 47 pf between pin 11 of IC47 and pin 7 of IC47 (component side).	RC network was added on the pHLDA line of the WDI to eliminate spurious noise on the line.
6 Supers. by #170.	84	1-9-80	Trace between IC2-13 & IC33-3 cut on component side. 560Ω between IC2-4 & IC2-13. 100 pf between IC2-13 & IC2-7. Supercedes ECO #52.	This circumvents the simultaneous occurance of $\overline{OE}$ low (pin 1) and latch low (pin 11) on chip 78 on the 64KZ. This problem would occasionally give 'failed compare' errors on Xfer of files.
7	105	2-6-80	Jump IC26-1 → IC26-16.	Pin 1 is the clear input to a 74LS174. The trace which should tie this to logic high (+5V) is missing.

Mod#	ECO#	Date Issued	CHANGE	REASON
8	139	3-3-80	3.3KΩ between IC12-12 & IC12-16.	Resistors in RN6 are pull-ups for the Z80 DMA chip (IC37). Adding the 3.3K will yield faster rise time on $\overline{\text{BUSRQ}}$ (pin 15, IC37). $\overline{\text{BUSRQ}}$ is connected to address line A2 of the DMACTL PROM (pin 12, IC12). The faster rise time provides more reliable operation of this PROM.
9	170	3-31-80	This supercedes ECO #84. Cut trace between IC19-3 & IC32-9 on the pin side. Jump IC19-8→IC32-9 on the pin side. Remove RC network (if installed) at IC2-4,13,7. (Mounted on IC2 itself). Jump IC2-4→IC2-13.	This eliminates a race condition between the outputs of IC19-3 and IC32-3. It also eliminates the glitch on PDBIN without the need for RC network at IC2-4,13,7.
10	254 269 316	5-21-80 5-30-80 7-7-80	Use Fairchild parts only, for transistors 2N3640 & 2N3646. Should already be on boards. If FAIRCHILD is unavailable, use NATIONAL for alternates.	Only Fairchild parts will work properly on the WDI board. National is 2'nd preference.
11	357	8-7-80	Replace metal screws & washers with nylon screws & washers, at the locations indicated: IC54-7905CT	This regulator's heatsink is electrically hot. Nylon hardware will alert users to this effect.