MODIFICATION LEVEL SUMMARY				
Product Type		64KZ-II D1 Revision Date	August 1, 1983	
Mod Level Released  1 4/2/82		Type of Change	Reason For Change  The 470 PF will lenghten the interval between the DMA board disable signal and the first SMI signal from 25us to 80us. For SDI DMA and general operation with WAIT states added.	
		Superceded by ML2. Change C79 from .001 PF to 470 PF Mono. Change C121 from 470 PF to .001 PF Mono.		
,	4/23/82	On the component side, cut the trace from IC2 pin 1 and jump IC2 pin 9; put back the 560 ohm resistor (R3, P/N 001-0015).  This avoides item 1 of ML 1 above	Since the 8us refresh counter is not cleared, the DPU in its 68000 mode can queue up a refresh request which can be clocked out just after the first request, thus locking up the curcuit. If the flip-flop clocked by the counter (IC2 pins 1-6) is kept "cleared" (jumping lin 1 to pin 9) the queued up refresh request will be held off until the proper time. This also corrects the SDI Host DMA problem.	
	,			
	a <sub>c</sub>			

MODIFICATION LEVEL SUMMARY 64KZ-II August 1, 1983 Product Type \_ Revision\_ Date Issued. Page\_ Mod Date Type of Change Reason For Change Level Released 1 3/19/82 On the solder side: Artwork corrections. 1.) Jump IC35 Pin 14 to adjacent +5V trace 2.) Jump IC54 Pin 2 to IC43 Pin 2. 3.) Jump CN6 Pin 1 to adjacent ground trace. 4.) Jump RN6 Pin 1 to top plate-through hole of R14. 5.) Scrape solder mask off top hole of D3. 6.) CN6 should be 100 PF (005-0021). R13 should be 2.2K ohm (001-0021).

Cromemco.

	VIOLICITIC					
Product Type		64KZ MODFIGATION DEEVEL SUMMARY August 1, 1983 1 1  Revision Legend: J2 Date Issued Page of				
Mod Level	Date Released	Type of Change	Reason For Change  Not needed. Delay line is now used.			
1	2/18/81	Delete 20 Mhz Crystal, 026-0002, from board.				
2	6/1/81	On solder side, <u>cut trace</u> and <u>jump</u> the two feedthrough holes.	This will route sOUT through the deglitch ing RC network (RN5 & C69) to IC59-10. Noise on sOUT taken directly off the bus could generate an invalid bank select pulse to IC8-9, causing the system to crash, when writing to memory addresses with lower addresses of 40H (also the bank select port).			
3	11/24/81	On the solder side:  Cut the MEMDISBL jumper, shown as point A on artwork.  Jump point A (Bus side) to IC23 pin 5.  Jump IC23 pin 4 to IC40 pin 3.  Jump point A (Bus side to IC23 pin 5.  Jump IC36 pin 6 to IC3 pin 2.  Jump IC36 pin 4 to IC36 pin 14.  On the component side:  Pull pin 1 of IC59 & jump to IC23 pin 6.  Pull pin 2 of IC3 & jump to IC36 pin 3.	This mod allows the 64KZ to be properly enabled and disabled for all operations. However, it will, in effect, create a new Board (64KZ-SDI, 520-0120) to be used only in SDI systems to replace the 64KZ Rev. Jl in a CDOS system (voiding ECO 776, ML 3 on the 48KTP) or a 64KZ Rev. Jl in the sam bank as the 48KTP's in a CROMIX system.			

D	roduct Type	64KZ MODIFICATION LEVEL SU			
Mod Date Level Released		Type of Change	Reason For Change		
10	6/1/81	On solder side, <u>cut trace</u> and <u>jump</u> the two feedthrough holes as shown.	This will route sOUT through the deglitch ing RC network (RN5 & C69) to IC59-10. Noise on sOUT taken directly off the bus could generate an invalid bank select pulse to IC8-9, causing the system to crash, when writing to memory addresses with lower addresses with lower addresses of 40H (also the bank select port).		

## MODIFICATION LEVEL SUMMARY

P	roduct Type _	Revision Da	Issuedof		
Mod Level	Date Released	64KZ J,Jl (contd.) Type of Change	August 1, 1983 2 3 Reason For Change		
6 ]	0/27/80	Change R21 from 330ohm resistor to 1K resistor. Change R7 & R8 from 2.2K res. to 680ohm resistors.	IC25 (a 74LS25 part) fanout exceeded. The IC tries to sink 17mA w/c. Stiffer pullups (faster risetimes on bank select on bank select circuit).		
7	8/20/80	Remove IC17, R26, R27, L1 and C24. Replace IC55 with the delay line package (from Bel Fuse).  Delete crystal.  Remove IC17 socket.	All control signals (internal to the 64KZ are synchronized with the start of any cycle eniminating the 50 nsec jitter generated by the asynchronous on board clock.  In the worst case, it makes each cycle faster by 30nsec.  Not needed.		
8 1	1/12/80	Change IC76 from a 74S374 to a 54S374.	The failure rate of 74L374's in this application is high as it runs hot. Test jig measurements indicate that the 54S374's will alleviate this component as a source of failure.		
9 1	2/12/80	Replace R4 & R5 180ohm resistors with 470ohm resistors.	The LS outputs at IC8 (a 399) could not pull down the diode resistor network in the worst case (which would give erroneous indication of bank activity). The LED's will be dimmer but acceptable.		

Cromemco'

MODIFICATION LEVEL SUMMARY 64KZ August 1, 1983 Revision\_ Product Type \_ Date Issued Page\_ \_ of \_\_\_\_ Mod Date Type of Change Reason For Change Level Released 1 Change IC77 from 74LS374 to 74LS373. 8/20/80 Considering a worst case ZPU-data from the ZPU (in a write cycle) is not stable on the rising edge of the clock to IC77, causing incorrect data to be written to the memory. Using a transparent flip-flop gives more time for this data to stablize since it is only sampled when CAS goes low. 2 8/20/80 Change R12 from 2.7 to 4.7K. To quarantee, that on reset, IC23-12 is pulled to a valid low. 3 8/20/80 Change IC56 from 74LS14 to 74S04. IC56 was used incorrectly in the Johnson Change R36 from 820ohm to 100ohm. counter and had a fanout problem. IC56 Change R37 from 1.8Kohm to 390ohm. was replaced by S04 and corresponding Change C82 from 330pf to 1Kpf. changes in R-C values were made to compensate for thia change since two gates of IC56 are also used in the DMA control circuitry. 4 8/20/80 Change Cl3 from 100pf to 220pf and Rl0 R-C network changed to conform with the from 240ohm to 100ohm. worst case Schottky input characteristics. Change Rll from 270ohm to 150ohm. Change R9 from 470ohm to 220ohm. Change R35 from 270ohm to 220ohm and C81 from 220pf to 330pf. Change C59 from 220pf mono cap to 470pf 5 9/9/80 Compatibility with 48KTP: This RC fix mono cap. slows down the start of an M-1 cycle by 18ns (21ns to 39ns propogation delay from IC20-5 to IC21-6) so that MEMDISABLE will be clocked in when valid at the 74LS175, IC41.

MODIFICATION LEVEL SUMMARY  August 1, 1983 1				1 1		
Product Type			Revision	Date Issue		Pageof
Mod Level	Date Released		Type of Change		Reason Fo	Change
	1/24/83	Pin 5 and to ICl Pic 2) Solder sin to IC3 Pic of RN1).  3) Solder a	de: Cut traces from Rnl Pin 2. Jump Rnn 5. de: Cut trace from n 8 (unnecessary was 47 PF monolithic can) from IC2 Pin 2 to	N1 Pin 2 2) RN1 Pin 4 3) ith Rev A 3) apacitor	Reduces crosstalk impedance error si Corrects feedback response. Improves hysteresi bottom comparator rising edge.	gnal. loop frequency s at the sawtooth
,	2/28/83	Pin 1. 2.) Solder s IC14 Pin	Side: Jump IC14 Pin	a 2 to c	everts the clock into set-up time violate ausing write errors	
3	3/15/83	2.Add a jumper	ECO 1517 above is n r from C59 (above g side of L3.		Rev A. of RN1 (003 Artwork correction	