BOARD MODIFICATIONS for WDI REV E1

ML- 9
9-25-80 (.31C)

Mod#	ECO#	Date Issued	CHANGE	REASON
1	55	9-16-79	Cut pin 4 of 34 pin connector.	A polarizing key will be added to the WDI cable attached to this connector.
2	76	12-17-79	R17 must be 100Ω, not 680Ω.	Need for systems of ≥5 memory cards.
3	81	1-9-80	Jump IC18-7 → IC19-7.	Missing artwork.
4 Superc. by #170.	84	1-9-80	Cut trace to IC2-4, pin side. Insert 560Ω between IC2-4 & IC2-13. Insert 100pf between IC2-13 & IC2-7.	This circumvents the simultaneous occurance of $\overline{OE}$ low (pin 1) and latch low (pin 11) on chip 78 on the 64KZ. This problem would occasionally give 'failed compare' errors on transfer of files.
5	105	2-6-80	Jump IC26-1 → IC26-16.	Missing trace. Pin 1 (the clear input to a 74LS174) should be tied to logic high (+5V).
6	139	3-3-80	Insert 3.3KΩ between IC12-12 &IC12-16 OR Change RN6 from 10K to 2.7KΩ.	Resistors in RN6 are pull-ups for the Z80 DMA chip (IC37). Adding the 3.3K, or changing all the RN values to 2.7K will yield faster rise time on $\overline{BUSRQ}$ (pin 15, IC37). $\overline{BUSRQ}$ is connected to address line A2 of the DMACTL PROM (pin 12, IC12). The faster rise time provides more reliable operation of this PROM.
7	170	3-31-80	This supercedes ECO #84. Cut trace between IC19-3 & IC32-9 on the pin side. Jump IC19-8 → IC32-9 on the pin side. Remove RC network (if installed) at IC2-4,13,7 (mounted on IC2 itself). Jump IC2-4 → IC2-13 on pin side, if cut.	This eliminates a race condition between the outputs of IC19-3 and IC32-3. It also eliminates the glitch on PDBIN without the need for RC network at IC2-4,13,7.